

Abstract

A semiconductor device for refreshing data stored in a memory device includes a cell area having $N+1$ number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a tag block having $N+1$ number of unit tag blocks, each storing at least one physical cell block address denoting a row address storing a data; and a control block for controlling the tag block and the predetermined cell block table for refreshing the data in the plurality of unit cells coupled to a word line in response to the physical cell block address.